a 3 carrying out a second heat treatment at a temperature of 900 to 1200°C.

REMARKS

The above amendment is made to correct the misidentification of the present application as a “divisional” -- it is a continuation -- and to more specifically set forth the invention that is the subject of the application.

Respectfully submitted,

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Attorney Docket No.: SEL 139 DIV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Shunpei Yamazaki et al.)
)
Serial No.: 09/808,162)
)
Filed: March 13, 2001)
)
For: Method For Fabricating A Semiconductor Device)
)

Commissioner for Patents
Washington D.C. 20231

ATTACHMENT

CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation [divisional] of copending U.S. Application Serial No. 09/386,782 filed on August 31, 1999.

1. (Amended) A method of fabricating a semiconductor device, said method comprising the steps of:

preparing a single crystal semiconductor substrate having a main surface of a {110} surface;

forming an oxide layer in the single semiconductor substrate;

[forming] adding hydrogen into the single semiconductor substrate from a side of the main surface through the oxide layer to form a hydrogen-containing layer [at a predetermined depth] in [a] the single crystal semiconductor substrate [having a main surface of a {110} plane];

bonding the single crystal semiconductor substrate and a supporting substrate to each other;

separating the single crystal semiconductor substrate by a first heat treatment along the hydrogen-containing layer;

[carrying out a second heat treatment at a temperature of 900 to 1200°C;]

polishing a single crystal semiconductor layer remaining on the supporting substrate and having a main surface of a {110} plane; and

forming [a plurality of TFTs each having] an active layer of a thin film transistor by using the single crystal semiconductor layer.

2. (Amended) A method of fabricating a semiconductor device, said method comprising the steps of:

preparing a single crystal semiconductor substrate having a main surface of a {110} surface;

first oxidizing the single crystal semiconductor substrate [forming] to form a porous semiconductor layer [by anodic oxidation of a single crystal semiconductor substrate having a main surface of a {110} plane];

carrying out a first heat treatment [to] on the porous semiconductor layer in a reducing atmosphere;

carrying out an epitaxial growth of a first single crystal semiconductor layer having a main surface of a {110} plane on the porous semiconductor layer;

second oxidizing the first single crystal semiconductor layer to form an oxide layer, wherein a remaining portion in the first single crystal semiconductor layer which is not oxidized in the second oxidizing step is defined as a second single crystal semiconductor layer;

bonding the single crystal semiconductor substrate and a supporting substrate to each other;

[carrying out a second heat treatment at a temperature of 900 to 1200°C;]

polishing the single crystal semiconductor substrate until the porous semiconductor layer is exposed;

removing the porous semiconductor layer to expose the second single crystal semiconductor layer; and

forming [a plurality of TFTs each having] an active layer of a thin film transistor by using the single crystal semiconductor layer [on] over the supporting substrate.

3. (Amended) A method of fabricating a semiconductor device, said method comprising the steps of:

preparing a single crystal semiconductor substrate having amain surface of a {110} surface;

adding oxygen ions into the single semiconductor substrate from a side of the main surface [forming] to form an oxygen-containing layer [at a predetermined depth] in [a] the single crystal semiconductor substrate [having a main surface of a {110} plane];

converting the oxygen-containing layer into a buried [insulating] oxide layer by a heat treatment, wherein a single crystal semiconductor layer having a main surface of a {110} plane remains on the buried oxide layer; and

[forming a plurality of TFTs each having] patterning the single crystal semiconductor layer to form an active layer of a thin film transistor [a single crystal semiconductor layer having a main surface of a {110} plane on the buried insulating layer].